AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A clock control system comprising:

a CPU;

a peripheral functional block for said CPU;

a frequency multiplication circuit which multiplies a frequency of an input system clock and outputs the multiplied system clock;

a first frequency division circuit which divides a frequency of a signal output from said frequency multiplication circuit to generate a first clock to be supplied to said CPU;

a second frequency division circuit which divides the frequency of the signal output from said frequency multiplication circuit to generate a second clock to be supplied to said peripheral functional block; and

clock control means for changing a frequency multiplication ratio of said frequency multiplication circuit to 1/N ~~(positive integer)~~ and then changing a frequency division ratio of said second frequency division circuit ~~arranged on an input stage of said peripheral functional block~~ to 1/N in order to set said CPU to a low-power consumption mode using no first clock,

wherein N is a positive integer.

2. (currently amended): A system according to claim 1, wherein in order to cancel the low-power consumption mode of said CPU, said clock control means changes N times the frequency division ratio of said second frequency division circuit ~~arranged on the input stage of said peripheral functional block,~~ and then changes N times the frequency multiplication ratio of said frequency multiplication circuit.

3. (currently amended): A clock control method in a clock control system ~~which has~~, the clock control system comprising a CPU, a peripheral functional block for the CPU, and a frequency multiplication circuit and a plurality of frequency division circuits that generate clocks to be supplied to the CPU and the peripheral functional block, ~~and in which~~ wherein a frequency of an input system clock is multiplied by the frequency multiplication circuit and divided by the frequency division circuits, and clocks are supplied to the CPU and the peripheral functional block, the method comprising, in order to set the CPU to a low-power consumption mode using no CPU clock:~~,~~ ~~the step of~~

changing a frequency multiplication ratio of the frequency multiplication circuit to 1/N; ~~(positive integer),~~ and ~~the subsequent step of~~

subsequently changing a frequency division ratio of the frequency division circuit arranged on an input stage of the peripheral functional block to 1/N,

wherein N is a positive integer.

4. (currently amended): A method according to claim 3, further comprising:~~,~~

in order to cancel the low-power consumption mode of the CPU, ~~the step of~~ changing N times the frequency division ratio of the frequency division circuit arranged on the input stage of the peripheral functional block;~~,~~ and ~~the subsequent step of~~

subsequently changing N times the frequency multiplication ratio of the frequency multiplication circuit.

5. (currently amended): A clock control method in a clock control system, the clock control system comprising ~~which has~~ a CPU, a peripheral functional block for the CPU, a frequency multiplication circuit and a plurality of frequency division circuits that generate clocks to be used for the CPU and the peripheral functional block, and control means for controlling the CPU, the frequency multiplication circuit, and the frequency division circuits, ~~and in which~~ wherein a frequency of an input system clock is multiplied by the frequency multiplication circuit, a signal output from the frequency multiplication circuit is input to the plurality of frequency division circuits, a frequency of the output signal is divided by a first frequency division circuit to supply the output signal as a CPU clock to the CPU, and the frequency of the signal output from the frequency multiplication circuit is divided by a second frequency division circuit to supply the output signal as a peripheral functional block clock to the peripheral functional block, said method comprising, in order to set the CPU to a low-power consumption mode using no CPU clock;~~,~~ ~~the step of~~

changing a frequency multiplication ratio of the frequency multiplication circuit to 1/N ~~(positive integer)~~ via the control means;~~,~~ and ~~the subsequent step of~~

subsequently changing a frequency division ratio of the second frequency division circuit arranged on an input stage of the peripheral functional block to 1/N via the control means,

wherein N is a positive integer.

6. (currently amended): A method according to claim 5, further comprising:~~,~~

in order to cancel the low-power consumption mode of the CPU, ~~the step of~~ changing N times the frequency division ratio of the second frequency division circuit arranged on the input stage of the peripheral functional block via the control means;~~,~~ and ~~the subsequent step of~~

subsequently changing N times the frequency multiplication ratio of the frequency multiplication circuit via the control means.

7. (currently amended): A clock control method in a clock control system, the clock control system comprising ~~which has~~ a CPU, a peripheral functional block for the CPU, a frequency multiplication circuit and a plurality of frequency division circuits that generate clocks to be used for the CPU and the peripheral functional block, and control means for controlling operations of the frequency multiplication circuit and the frequency division circuits, ~~and in which~~ wherein a frequency of an input system clock is multiplied by the frequency multiplication circuit, the multiplied frequency is input to the plurality of frequency division circuits connected as first and second frequency division circuits to input stages of the CPU and the peripheral functional block, a frequency of a signal output from the frequency multiplication circuit is divided by the first frequency division circuit to supply the signal as a CPU clock to the CPU, the

frequency of the signal output from the frequency multiplication circuit is divided by the second frequency division circuit to supply the signal as a peripheral functional block clock to the peripheral functional block, said method comprising, in order to set the CPU to a low-power consumption mode;, ~~the step of~~

confirming whether the peripheral functional block keeps operating, on the basis of whether the control means has received a second clock stop enable signal output from the peripheral functional block ~~when~~ if the control means receives a first clock stop enable signal output from the CPU;,

~~the step of~~ determining that the peripheral functional block keeps operating ~~when~~ if the control means has not received the second clock stop enable signal output from the peripheral functional block;,

~~the step of~~ changing a frequency multiplication ratio of the frequency multiplication circuit to 1/N ~~(positive integer)~~ via the control means;, and ~~the subsequent step of~~

subsequently changing a frequency division ratio of the second frequency division circuit arranged on the input stage of the peripheral functional block to 1/N via the control means,

wherein N is a positive integer.

8. (currently amended): A method according to claim 7, further comprising, in order to cancel the low-power consumption mode of the CPU;, ~~the step of~~

confirming whether the peripheral functional block keeps operating, on the basis of whether the control means has received the second clock stop enable signal output from the

peripheral functional block ~~when~~ if the control means does not receive the first clock stop enable signal output from the CPU;, ~~the step of~~

determining that the peripheral functional block keeps operating ~~when~~ if the control means has not received the second clock stop enable signal output from the peripheral functional block;, ~~the step of~~

changing N times the frequency division ratio of the second frequency division circuit arranged on the input stage of the peripheral functional block via the control means;, and ~~the subsequent step of~~

subsequently changing N times the frequency multiplication ratio of the frequency multiplication circuit via the control means.